Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor device comprising:

a MIS transistor formed on a semiconductor substrate,

wherein said semiconductor substrate is an epitaxial semiconductor substrate having an expitaxial region formed by epitaxial growing silicon on a silicon substrate ~~using Cz method; and~~

said MIS transistor includes a gate electrode formed above said epitaxial region with a gate insulating film sandwiched therebetween and a diffusion layer formed in said expitaxial region, by using a dopant ion having a relatively large mass number, and

~~wherein~~ said diffusion layer is formed shallower than said epitaxial region.

2. (Original) The semiconductor device of Claim 1, wherein said epitaxial region has a <110>-oriented zone axis.

3. (Previously Presented) The semiconductor device of Claim 1, wherein said diffusion layer is formed by using, as said dopant ion, an indium ion.

4. (Currently Amended) The semiconductor device of Claim 1, wherein said diffusion layer corresponds to a pocket diffusion layer of [[a]] said MIS ~~semiconductor device~~ transistor, and said MIS ~~semiconductor device~~ transistor includes:

~~a gate electrode formed above said epitaxial region with a gate insulating film sandwiched therebetween;~~

a source/drain diffusion layer of a first conductivity type formed in a source/drain region of said epitaxial region at a distance from a region below a side face of said gate electrode;

an extension diffusion layer of the first conductivity type formed in said epitaxial region between said source/drain diffusion layer and said region below the side face of said gate electrode and having shallower junction than said source/drain diffusion layer; and

said pocket diffusion layer of a second conductivity type formed in said epitaxial region under said extension layer.

5. (Previously Presented) The semiconductor device of Claim 4, wherein said extension diffusion layer is formed by using an antimony ion as a dopant.

6. (Currently Amended) A semiconductor device comprising:

a MIS transistor formed on a semiconductor substrate,

wherein [[a]] said semiconductor substrate composed of silicon and having a main surface of {110}- orientation[[;]], and

said MIS transistor includes a gate electrode formed above said semiconductor substrate with a gate insulating film sandwiched therebetween and a diffusion layer formed, by using a dopant ion having a relatively large mass number, in said semiconductor substrate.

7. (Previously Presented) The semiconductor device of Claim 6, wherein said diffusion layer is formed by using, as said dopant ion, an indium ion.

8. (Currently Amended) The semiconductor device of Claim 6, wherein said diffusion layer corresponds to a pocket diffusion layer of [[a]] said MIS ~~semiconductor device~~ transistor, and said MIS ~~semiconductor device~~ transistor includes:

~~a gate electrode formed above said semiconductor substrate with a gate insulating film sandwiched therebetween;~~

a source/drain diffusion layer of a first conductivity type formed in a source/drain region of said semiconductor substrate at a distance from a region below a side face of said gate electrode;

an extension diffusion layer of the first conductivity type formed in said semiconductor substrate between said source/drain diffusion layer and said region below the

side face of said gate electrode and having shallower junction than said source/drain diffusion layer; and

said pocket diffusion layer of a second conductivity type formed in said semiconductor substrate under said extension diffusion layer.

9. (Previously Presented) The semiconductor substrate of Claim 8,

wherein said extension diffusion is formed by using an antimony ion as a dopant.

10. (Withdrawn) A method for fabricating a semiconductor device comprising:

a step of forming a heavily-doped diffusion layer by implanting a dopant ion having a relatively large mass number into an epitaxial region of silicon included in at least an upper portion of an epitaxial semiconductor substrate.

11. (Withdrawn) The method for fabricating a semiconductor device of Claim 10,

wherein said epitaxial region has a <110>-oriented zone axis.

12. (Withdrawn) The method for fabricating a semiconductor device of Claim 10,

wherein said heavily-doped diffusion layer is formed by using, as said dopant ion, an indium ion at a dose of $5 \times 10^{13}/cm^{-2}$ or more.

13. (Withdrawn) The method for fabricating a semiconductor device of Claim 10,

wherein said heavily-doped diffusion layer corresponds to a pocket heavily-doped diffusion layer of a MIS semiconductor device, and

the method for fabricating said MIS semiconductor device includes the steps of:

forming a gate electrode above said epitaxial region with a gate insulating film sandwiched therebetween;

forming a first dopant layer to be used as said pocket heavily-doped diffusion layer by implanting a first dopant of a first conductivity type corresponding to said dopant ion into said epitaxial region with said gate electrode used as a mask;

forming a second dopant layer to be used as an extension heavily-doped diffusion layer by implanting a second dopant of a second conductivity type into said epitaxial region

to have shallower junction than said first dopant layer with said gate electrode used as a mask; and

forming a sidewall on a side face of said gate electrode, and forming a third dopant layer to be used as a source/drain heavily-doped diffusion layer by implanting a third dopant of the second conductivity type into said epitaxial region to have deeper junction than said second dopant layer with said gate electrode and said sidewall used as a mask.

14. (Withdrawn) The method for fabricating a semiconductor device of Claim 13, further comprising a step of forming a fourth dopant layer to be used as a channel diffusion layer by implanting a fourth dopant of the first conductivity type into said epitaxial region before forming said gate electrode.

15. (Withdrawn) The method for fabricating a semiconductor device of Claim 13, wherein said second dopant is an antimony ion.

16. (Withdrawn) A method for fabricating a semiconductor device comprising:

a step of forming a heavily-doped diffusion layer by implanting a dopant ion having a relatively large mass number into a semiconductor substrate under conditions for suppressing dislocation loop defects caused in said semiconductor substrate.

17. (Withdrawn) The method for fabricating a semiconductor device of Claim 16, wherein said heavily-doped diffusion layer is formed by using, as said dopant ion, an indium ion at a dose of $5 \times 10^{13}/cm^{-2}$ or more.

18. (Withdrawn) The method for fabricating a semiconductor device of Claim 16, wherein said dopant ion is implanted at a current density of approximately 100 $\mu A/cm^2$ or less.

19. (Withdrawn) The method for fabricating a semiconductor device of Claim 16, wherein said dopant ion is implanted at an angle of approximately 30 degrees or more against a vertical direction to a substrate surface of said semiconductor substrate.

20. (Withdrawn) The method for fabricating a semiconductor device of Claim 16, wherein said heavily-doped diffusion layer corresponds to a pocket heavily-doped diffusion layer of a MIS semiconductor device, and

the method for fabricating said MIS semiconductor device includes the steps of:

forming a gate electrode above said semiconductor substrate with a gate insulating film sandwiched therebetween;

forming a first dopant layer to be used as said pocket heavily-doped diffusion layer by implanting a first dopant of a first conductivity type corresponding to said dopant ion into said semiconductor substrate with said gate electrode used as a mask;

forming a second dopant layer to be used as an extension heavily-doped diffusion layer by implanting a second dopant of a second conductivity type into said semiconductor substrate to have shallower junction than said first dopant layer with said gate electrode used as a mask; and

forming a sidewall on a side face of said gate electrode, and forming a third dopant layer to be used as a source/drain heavily-doped diffusion layer by implanting a third dopant of the second conductivity type into said semiconductor substrate to have deeper junction than said second dopant layer with said gate electrode and said sidewall used as a mask.

21. (Withdrawn) The method for fabricating a semiconductor device of Claim 20, further comprising a step of forming a fourth dopant layer to be used as a channel diffusion layer by implanting a fourth dopant of the first conductivity type into said semiconductor substrate before forming said gate electrode.

22. (Withdrawn) The method for fabricating a semiconductor device of Claim 20, wherein said second dopant is an antimony ion.

23. (Withdrawn) A method for fabricating a semiconductor device comprising:

a step of forming a heavily-doped diffusion layer by implanting a dopant ion having a relatively large mass number into a semiconductor substrate having a <110>-oriented zone axis.

24. (Withdrawn) The method for fabricating a semiconductor device of Claim 23, wherein said heavily-doped diffusion layer is formed by using, as said dopant ion, an indium ion at a dose of $5 \times 10^{13}/cm^{-2}$ or more.

25. (Withdrawn) The method for fabricating a semiconductor device of Claim 23, wherein said heavily-doped diffusion layer corresponds to a pocket heavily-doped diffusion layer of a MIS semiconductor device, and

the method for fabricating said MIS semiconductor device includes the steps of:

forming a gate electrode above said semiconductor substrate with a gate insulating film sandwiched therebetween;

forming a first dopant layer to be used as said pocket heavily-doped diffusion layer by implanting a first dopant of a first conductivity type corresponding to said dopant ion into said semiconductor substrate with said gate electrode used as a mask;

forming a second dopant layer to be used as in extension heavily-doped diffusion layer by implanting a second dopant of a second conductivity type into said semiconductor substrate to have shallower junction than said first dopant layer with said gate electrode used as a mask; and

forming a sidewall on a side face of said gate electrode, and forming a third dopant layer to be used as a source/drain heavily-doped diffusion layer by implanting a third dopant of the second conductivity type into said semiconductor substrate to have deeper junction than said second dopant layer with said gate electrode and said sidewall used as a mask.

26. (Withdrawn) The method for fabricating a semiconductor device of Claim 25, further comprising a step of forming a fourth dopant layer to be used as a channel diffusion layer by implanting a fourth dopant of the first conductivity type into said semiconductor substrate before forming said gate electrode.

27. (Withdrawn) The method for fabricating a semiconductor device of Claim 25, wherein said second dopant is an antimony ion.

28. (Previously Presented) The semiconductor device of Claim 3, wherein said diffusion layer is formed by said indium ion at a dose of $5 \times 10^{13}/cm^2$ or more.

29. (Previously Presented) The semiconductor device of Claim 2, wherein said diffusion layer is formed by using, as said dopant ion, an indium ion.

30. (Currently Amended) The semiconductor device of Claim 3, wherein said diffusion layer corresponds to a pocket diffusion layer of [[a]] said MIS ~~semiconductor device~~ transistor, and said MIS ~~semiconductor device~~ transistor includes:

~~a gate electrode formed above said epitaxial region with a gate insulating film sandwiched therebetween;~~

a source/drain diffusion layer of a first conductivity type formed in a source/drain region of said epitaxial region at a distance from a region below a side face of said gate electrode;

an extension diffusion layer of the first conductivity type formed in said epitaxial region between said source/drain diffusion layer and said region below the side face of said gate electrode and having shallower junction than said source/drain diffusion layer; and

said pocket diffusion layer of a second conductivity type formed in said epitaxial region under said extension diffusion layer.

31. (Previously Presented) The semiconductor device of Claim 30, wherein said extension diffusion layer is formed using an antimony ion as a dopant.

32. (Cancelled).

33. (Cancelled).

34. (Previously Presented) The semiconductor device of Claim 1, wherein said diffusion layer is formed by using, as said dopant ion, an antimony ion.

35. (Previously Presented) The semiconductor device of Claim 7, wherein said diffusion layer is formed by said indium ion at a dose of $5 \times 10^{13}/cm^2$ or more.

36. (Currently Amended) The semiconductor device of Claim 7, wherein said diffusion layer corresponds to a pocket diffusion layer of [[a]] said MIS ~~semiconductor device~~ transistor, and said MIS ~~semiconductor device~~ transistor includes:

~~a gate electrode formed above said semiconductor substrate with a gate insulating film sandwiched therebetween;~~

a source/drain diffusion layer of a first conductivity type formed in a source/drain region of said semiconductor substrate at a distance from a region below a side face of said gate electrode;

an extension diffusion layer of the first conductivity type formed in said semiconductor substrate between said source/drain diffusion layer and said region below the side face of said gate electrode and having shallower junction than said source/drain diffusion layer; and

said pocket diffusion layer of a second conductivity type formed in said semiconductor substrate under said extension diffusion layer.

37. (Previously Presented) The semiconductor device of Claim 36, wherein said extension diffusion layer is formed using an antimony ion as a dopant.

38. (Previously Presented) The semiconductor device of Claim 6, wherein said diffusion layer is formed by using, as said dopant ion, an antimony ion.

39. (New) The semiconductor device of Claim 1, wherein said diffusion layer is a channel diffusion layer formed below said gate electrode in said epitaxial region.

40. (New) The semiconductor device of Claim 3, wherein said diffusion layer is a channel diffusion layer formed below said gate electrode in said epitaxial region.

41. (New) The semiconductor device of Claim 1, wherein said diffusion layer is a pocket diffusion layer formed on both sides of said gate electrode in said epitaxial region.

42. (New) The semiconductor device of Claim 3, wherein said diffusion layer is a pocket diffusion layer formed on both sides of said gate electrode in said epitaxial region.

43. (New) The semiconductor device of Claim 7, wherein said diffusion layer is a channel diffusion layer formed below said gate electrode in said semiconductor substrate.

44. (New) The semiconductor device of Claim 7, wherein said diffusion layer is a pocket diffusion layer formed on both sides of said gate electrode in said semiconductor substrate.

45. (New) The semiconductor device of Claim 1, wherein said silicon substrate has a Cz crystal substrate formed by using Cz method.